AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate;

a polysilicon pattern formed on said semiconductor substrate via an insulation film, wherein said polysilicon pattern includes at least one doped gate electrode and at least one doped resistance element;

an interlayer insulation film formed on said semiconductor substrate so as to cover said polysilicon pattern; ~~and~~

a first silicon nitride film formed on said interlayer insulation film;

a metal interconnection layer pattern formed directly on said first silicon nitride layer; and ~~interlayer insulation film,~~

~~wherein said metal interconnection layer pattern carrying~~ a second silicon nitride film[[s]] formed directly ~~respectively~~ on a top surface~~, a bottom surface~~ and sidewall surfaces ~~thereof~~ of said metal interconnection layer pattern,

wherein said metal interconnection layer pattern is not an uppermost metal interconnection layer pattern.

2. (Canceled)

3. (Currently amended) The semiconductor device as claimed in claim 1 [[2]], wherein said first nitride film and said second nitride film have respective, different thicknesses.

4. (Currently amended) The semiconductor device as claimed in claim 1 [[2]], ~~wherein there is provided~~ further comprising a region wherein said first silicon nitride film and

said second silicon nitride film are removed except for said first silicon nitride film underlying said metal interconnection layer pattern.

5. (Currently amended) The semiconductor device as claimed in claim 1, ~~wherein said semiconductor device~~ further comprising[[es]] a p-channel MOS transistor having a gate electrode formed of said polysilicon pattern, wherein formation of said metal interconnection layer pattern, said first silicon nitride film and said second silicon nitride film ~~being~~ are suppressed in a region over said p-channel MOS transistor.

6. (Currently amended) The semiconductor device as claimed in claim 1, ~~wherein there is provided~~ further comprising a laminated film formed between said polysilicon pattern and said interlayer insulation film, said laminated film comprising consecutive lamination of an oxide film and a third silicon nitride film in a direction from said polysilicon pattern to said interlayer insulation film.

7. (Currently amended) The semiconductor device as claimed in claim 6, ~~wherein said semiconductor device~~ further comprising[[es]] a p-channel MOS transistor having a gate electrode of said polysilicon pattern, wherein said third silicon nitride film is ~~being~~ formed over said p-channel MOS transistor.

8. (Currently amended) A semiconductor device having a voltage divider circuit producing an output voltage by dividing a voltage supplied thereto,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance elements comprising a doped portion of a polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a first silicon nitride film formed on said interlayer insulation film;

a metal interconnection layer pattern being formed directly on said first silicon nitride layer; and ~~interlayer insulation film,~~

~~said metal interconnection layer pattern carrying~~ a second silicon nitride film[[s]] formed directly ~~respectively~~ on a top surface~~, a bottom surface~~ and sidewall surfaces ~~thereof~~ of said metal interconnection layer pattern,

wherein said metal interconnection layer pattern is not an uppermost metal interconnection layer pattern.

9. (Currently amended) A semiconductor device comprising:

a voltage divider circuit dividing a voltage supplied thereto and producing an output voltage;

a reference voltage generator supplying a reference voltage; and

a comparator circuit comparing said output voltage of said voltage divider circuit with said reference voltage of said reference voltage generator,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance elements comprising a doped portion of a polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a first silicon nitride film formed on said interlayer insulation film;

a metal interconnection layer pattern being formed directly on said first silicon nitride layer; and ~~interlayer insulation film,~~

~~said metal interconnection layer pattern carrying~~ a second silicon nitride film[[s]] formed directly ~~respectively~~ on a top surface~~, a bottom surface~~ and sidewall surfaces ~~thereof~~ of said metal interconnection layer pattern,

wherein said metal interconnection layer pattern is not an uppermost metal interconnection layer pattern.

10. (Currently amended) A semiconductor device, comprising:

an output driver controlling an output of an input voltage;

a voltage divider circuit dividing said output voltage and producing a divided voltage;

a reference voltage generator producing a reference voltage; and

a constant voltage generator having a comparator circuit comparing said divided voltage from said voltage divider circuit and said reference voltage from said reference voltage generator, said comparator circuit controlling said output driver in response to a result of comparison,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance elements comprising a doped portion of a polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a first silicon nitride film formed on said interlayer insulation film;

a metal interconnection layer pattern being formed directly on said first silicon nitride layer; and ~~interlayer insulation film,~~

~~said metal interconnection layer pattern carrying~~ a second silicon nitride film[[s]] formed directly ~~respectively~~ on a top surface~~, a bottom surface~~ and sidewall surfaces ~~thereof~~ of said metal interconnection layer pattern,

wherein said metal interconnection layer pattern is not an uppermost metal interconnection layer pattern.

11. (Currently amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a polysilicon pattern on a semiconductor substrate via an insulation film, wherein said polysilicon pattern includes at least one doped gate electrode and at least one doped resistance element;

forming an interlayer insulation film on the semiconductor substrate so as to cover the polysilicon pattern;

forming a first nitride film on the interlayer insulation film;

forming a metal interconnection layer pattern directly on the first nitride film; and

forming a second nitride film directly on the metal interconnection layer pattern and on portions of the first nitride film that are not covered by ~~so as to cover~~ the metal interconnection layer pattern,

wherein said metal interconnection layer pattern is not an uppermost metal interconnection layer pattern.

12. (Currently amended) The method as claimed in claim 11, further comprising the step, after said step of forming said second nitride film, of selectively removing said second nitride film and said first nitride film ~~selectively~~ from a predetermined area.